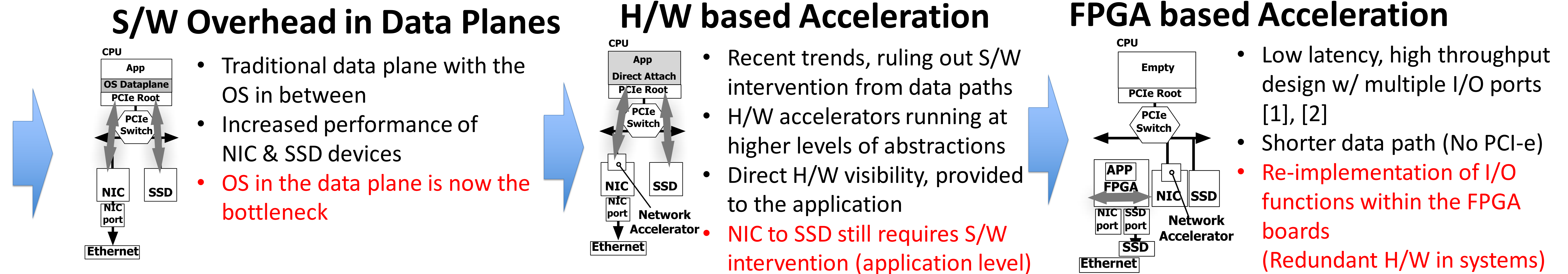


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Abstract

In this paper, we present a cost effective FPGA based data plane design which reuses existing I/O devices such as 10GbE NICs or NVM-e SSDs as data ingress and egress ports. We achieved this by building a FPGA based device driver logic which is capable of exploiting PCI-e point to point communication. FPGA H/W design support such as C based High Level Synthesis tools enabled us to implement complex device drivers within FPGAs. Our design avoids re-implementing the performance and stability of existing ASIC based commodity I/O devices, already installed in our systems, thus reducing data plane implementation costs.



Key Ideas: Enablers

PCI-express P2P Communication

- Exploit endpoint to endpoint communication to gain efficient data movement without S/W intervention

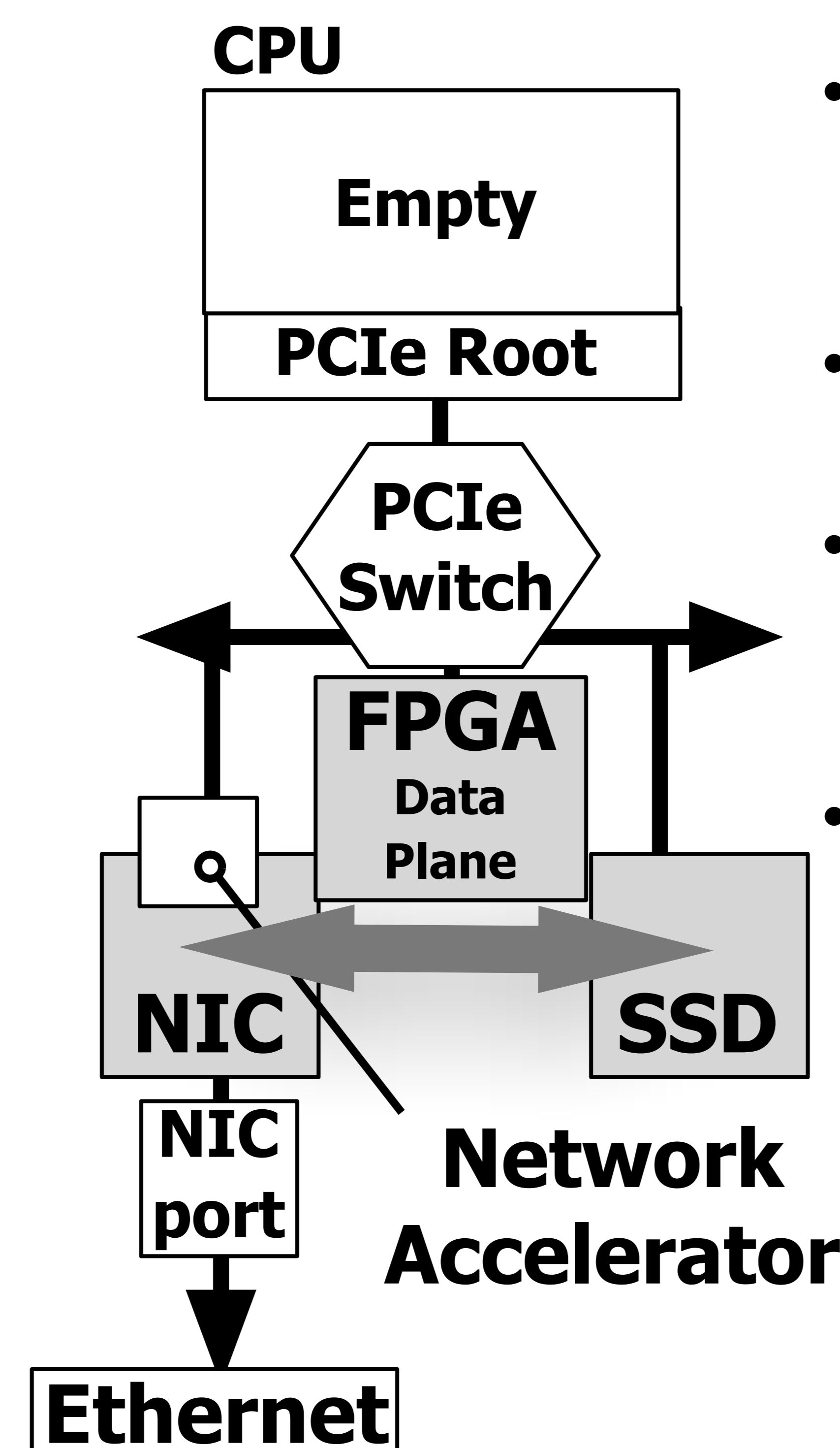
FPGAs + ASIC design

- FPGAs are now powerful, but we do not use them to implement I/O functions
- We already have high performance ASIC based controllers in our NICs & SSDs

High Level Synthesis (C/C++/SystemC)

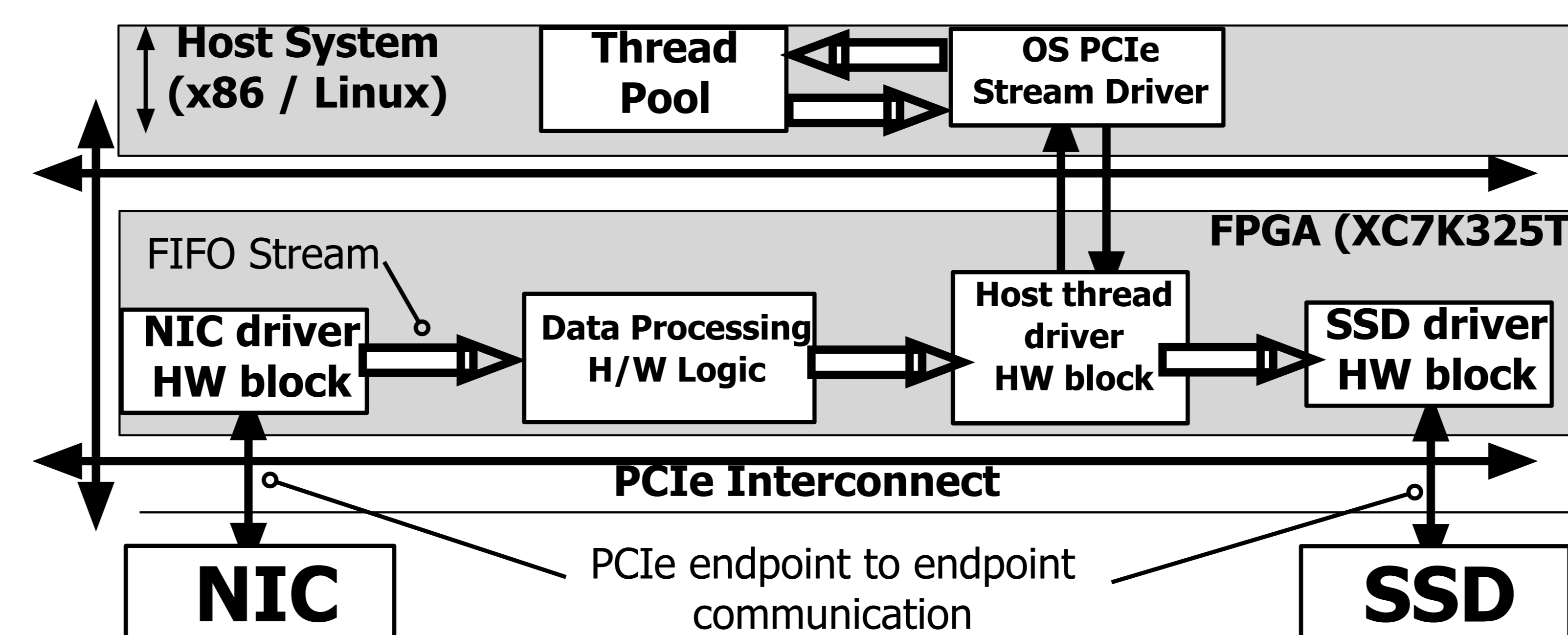
- P2P communication and control requires a device driver, but it should be in the FPGA
- Complexity of the implementation can be alleviated by high level design tools

Our Proposal: Reusing Existing Components



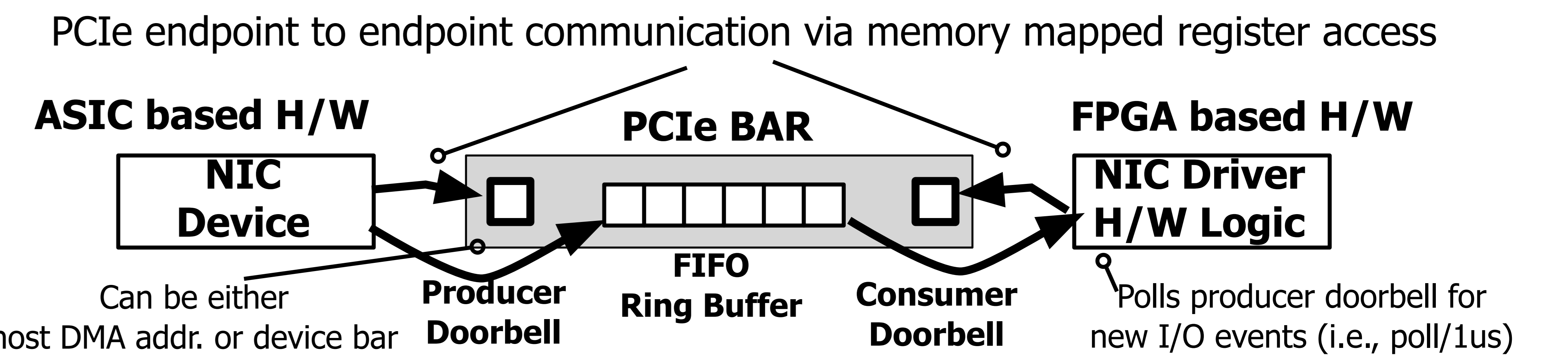
- FPGA based device to device data path acceleration: high level application specific operations are implemented
- Integrate pre-existing PCI-e interconnects and I/O devices in the system
- FPGA based device driver is implemented to perform device to device communication without host S/W intervention
- Control plane operations are performed by the OS software.

Data Path Design



Stream based data path design is used. A FIFO stream abstraction is used to glue data processing units. Data processing units can be H/W blocks or host side data processing threads.

OS Device Drivers running on FPGAs as H/W Logic



Device drivers on modern high performance I/O devices are implemented in a FIFO queue producer & consumer style. Identical to OS device drivers, but provides low latency and high throughput

Conclusion

In this work, we have proposed a cost effective FPGA based data plane which involves multiple I/O devices. Rather than re-implementing I/O functions within a single FPGA board, our proposal is to link pre-existing ASIC based I/O devices in the data path by exploiting PCI-e endpoint to endpoint communication from a PCI-e attached FPGA. By doing this, we aim to capture the superior performance of these ASIC based I/O devices and perform a cost effective FPGA based data plane acceleration at a more higher abstraction level.

References

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